

COMPARISON BETWEEN Si/SiO₂ AND InP/Al₂O₃ BASED MOSFETS

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Electron transport properties of InP-based MOSFET as a new channel material with Al₂O₃ as a high-*k* dielectric oxide layer in comparison with Si-based MOSFET are studied by the ensemble Monte Carlo simulation method in which the conduction band valleys in InP are based on three valley models with consideration of quantum effects (effective potential approach). I_d - V_d characteristics for Si-based MOSFET are in good agreement with theoretical and experimental results. Our results show that I_d of InP-based MOSFET is about 2 times that of Si-based MOSFET. We simulated the diagrams of longitudinal and transverse electric fields, conduction band edge, average electron velocity, and average electron energy for Si-based MOSFET and compared the results with those for InP-based MOSFET. Our results, as was expected, show that the transverse electric field, the conduction band edge, the electron velocity and the electron energy in a channel in the InP-based MOSFET are greater than those for Si-based MOSFET. But the longitudinal electric field behaves differently at different points of the channel.

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1. INTRODUCTION

A few years ago, miniaturization of transistors applied to the building of integrated circuits and microchips of smaller sizes was of interest to industry and researchers. Recently, it has been found that down-sizing Si-based MOSFETs is not sufficient for improving the device performance [1]. Therefore, in order to achieve a higher drive current, suppress the current leakage, minimize short channel effects, and also attain higher speeds, a new channel material has been considered [1–3]. III–V compound semiconductors like InP are applicable due to their higher electron mobility, higher electron saturation velocity ($2.5 \cdot 10^7$ cm/s in InP and $1 \cdot 10^7$ cm/s in Si), and a direct band gap [1–7]. InP has a lower intrinsic carrier concentration in comparison with Si, and this feature causes the InP

fabricated device to avoid thermally generated carriers at higher temperatures [8].

With this regard, designing an InP-based MOSFET of nanometer size and analyzing electron transport in it can be beneficial.

Rapid progress in electronic industry is indebted to simulation. Simulation reduces the huge cost of modeling and components design as well as the consumed time. With the increase in computer power in recent years, there are now more capabilities of simulation. It should be noted that the goal of simulation is not to reach more accurate diagrams for comparison, but to analyze the conditions and factors in experimental work [9, 10].

There are a few experimental results for regarding the use of InP as a channel semiconductor in MOSFET devices. The comparison has been accomplished for transistors of similar or close dimensions and semiconductors with similar properties. The limitation of InP experimental tests is related to the problems in making components because InP has a proper potential barrier in contacts [11, 12].

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In new designs of semiconductor components, besides replacing Si with III-V semiconductors, other applicable insulators except SiO₂ are used for the gate oxide layer.

Forming a high-quality gate dielectric on InP can help in making a high-speed transistor [2]. In 2003, a MOSFET on a III-V substrate with an Al₂O₃ gate dielectric deposited by atomic layer deposited (ALD) technique was reported for the first time [13]. Since then, this material has received great attention and Al₂O₃ is now a highly desirable deposited gate dielectric from the standpoint of both physical and electrical characteristics due to its high dielectric constant and breakdown field [2, 13–21]. Therefore, careful surface engineering can control the quality of a high-k/InP interface [2].

By the use of the Monte Carlo simulation method, Fischetti and Laux [22] analyzed physical and electrical properties of MOSFET with dimensions similar to the dimensions of our simulated transistor for Si and III-V semiconductors (especially, InP) at the temperature of 300 K and less. In this simulation, we obtained the values of the conduction band edge as well as the longitudinal and transverse electric field in each point of the channel. Moreover, by the use of Al₂O₃ as a high-*k* dielectric, we eliminated the problems of current leakage in MOSFETs based on III-V semiconductors as demonstrated in [22].

2. SIMULATION MODEL

An effective potential approach removes the need of directly solving the Schrödinger equation in MOSFETs with a very short channel length (below 100 nm). The most significant effect of this quantization is in distancing electrons from the interface [7, 23–25]. The ensemble Monte Carlo (EMC) simulation method for electron transport is realised by considering real two-dimensional (2D) space and the inverse three-dimensional space [26].

The electron energy and momentum also change due to the scattering process [7, 23, 27]. Therefore, without considering short-channel effects, it was expected that the drift velocity would decrease as the temperature increases [28, 29]. Computations were carried out with the three-valley model and the energy bands considered to have a nonparabolic band structure, with the electron scattering from lattice phonons taken into account. We have included the intervalley acoustic and optical phonon scattering. Furthermore, Coulomb scattering is ignored in our calculation. According to

Table. Band structure and material parameters used in the simulation [24–30]

		Si	InP
Effective mass	$m_\Gamma (m_0)$	—	0.082 ^a
$m_L (m_0)$	m_l	—	1.878 ^a
	m_t	—	0.153 ^a
$m_X (m_0)$	m_l	0.9163 ^b	1.321 ^a
	m_t	0.1905 ^b	0.273 ^a
Non-parabolicity, eV ⁻¹	Γ	—	0.83 ^c
	L	—	0.23 ^c
	X	0.5 ^a	0.38 ^c
Valley separation (Γ -L), eV	—	—	0.54 ^c
Valley separation (Γ -X), eV	—	—	0.775 ^c
Band gap energy, eV	1.1242 ^b	1.344 ^b	
Intrinsic carrier density, cm ⁻³	$1.45 \cdot 10^{16}$ ^d	$1.2 \cdot 10^{13}$ ^d	
Density, kg/m ³	2329.002 ^b	4810 ^b	
Sound velocity, m/s	9050 ^e	5130 ^c	
Acoustic deformation potential, eV	6.55 ^e	8.0 ^c	
Polar optical phonon energy, eV	0.062 ^a	0.0424 ^a	
Low-frequency dielectric constant ε_0	11.97 ^b	12.56 ^b	
High-frequency dielectric constant ε_∞	—	9.52 ^c	
Dielectric constant of Al ₂ O ₃		9.6 ^f	
Dielectric constant of SiO ₂		3.9 ^g	

^aFrom Ref. [24].

^bFrom Ref. [25].

^cFrom Ref. [26].

^dFrom Ref. [27].

^eFrom Ref. [28].

^fFrom Ref. [29].

^gFrom Ref. [30].

Moglestue [7], there are 6 and 8 possible destinations for intervalley scattering from the central valley to X and L valleys. Intervalley scattering in the L valley by the possible number of 1, 3, 3 transfer states is considered for three states of the g-process, f-process, and h-process. Intervalley scattering in the X valley by the possible number of 1 and 4 transfer states is related to two states of the g-process for opposite scattering and the f-process for other scatterings.

For analyzing high-energy electrons (with the energy above 1 eV) in high operating voltages (around 5 V according to Ref. [30]), a full-band Monte Carlo method is required. In this paper, the maximum electron energy is limited to 1 eV ($E_{max} = 1$ eV) in the operating voltages and hence the three-valley model of the Monte Carlo method for InP and the X valley model of the Monte Carlo method for Si are applicable.

The Monte Carlo method is well-known in simulating semiconductor components, and it has already been explained in detail in [7] and [27]. Therefore, we can avoid explaining relationships of the nonparabolicity coefficient or its influence on the energy band equation and we only mention its values in Table [31–37]. Material and band structure parameters used in simulation are shown in Table [31–37]. The time step and mesh size are the input parameters in the simulation. For determining the mesh size, we note that the lowest wavelength is the Debye length λ_D defined by Eq. (1),

$$\lambda_D = \left[\frac{\varepsilon \varepsilon_0 k_B T}{n e^2} \right]^{1/2}, \quad (1)$$

where $\varepsilon_0 = 8.8 \cdot 10^{-12} F/m$, k_B is Boltzmann constant, and T is the temperature [7]. Further, n is carrier density and for InP at room temperature with the carrier density of 10^{18} cm^{-3} , and the Debye length is about 42 Å. Therefore, the mesh size ($\Delta x = 2 \text{ nm}$, $\Delta y = 0.5 \text{ nm}$) for this simulation is considered. The third dimension of the device is considered along z for determining the number of intrinsic carriers in each cell. Therefore, the cell volume is obtained by multiplying the mesh size by the width of the device.

But the time step should be so low that the longest distance L_{max} that the carriers pass in this time Δt be less than the mesh size in Eq. (2):

$$L_{max} = V_{max} \Delta t. \quad (2)$$

We have chosen the time step $\Delta t = 1 \cdot 10^{-16} \text{ s}$, in which case L_{max} is less than 1.0 Å. The charge distribution and location of electrons in the channel are obtained by the use of the Monte Carlo simulation method. For solving the 2D Poisson equation, the incomplete lower upper decomposition method is used.

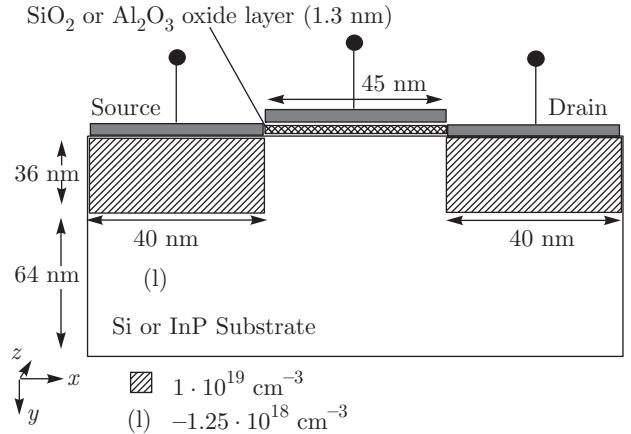


Fig. 1. Geometry of the simulated MOSFET

3. RESULTS

Figure 1 shows the MOSFET model used in this simulation. The MOSFET has an n -channel 40 nm in length and the device width along the z axis is 450 nm. The source and drain junctions are doped to $1 \cdot 10^{19} \text{ cm}^{-3}$. The channel and substrate are doped to $-1 \cdot 10^{18} \text{ cm}^{-3}$. This value should be logical because donor concentrations in most of the III–V semiconductors cannot be more than $2 \cdot 10^{19} \text{ cm}^{-3}$ [22]. By applying a gate voltage of 0.8 V and two drain voltages of 0.3 and 0.9 V, the diagrams of electron density, the longitudinal and transverse electric field, and the conduction band edge are drawn in different widths.

Figure 2 shows the longitudinal and transverse electric field and the conduction band edge-X position characteristics at the temperature of 300 K in the applied gate voltage $V_g = 0.8$ V. Having compared the two drain voltage of 0.3 and 0.9 V, we took InP-based MOSFET and Al_2O_3 as the oxide layer with Si-based MOSFET and SiO_2 as the oxide layer.

Figure 2 shows that 3 nm below the gate, the longitudinal electric field peak is negative and is close to the source, and the field peak is increased in this area as the drain voltage increases. Moreover, negative field values for InP-based MOSFET near the source are greater than those for Si-based MOSFET.

The effect of a negative longitudinal electric field E_x close to the source has been removed at lower latitudes and with receding from the gate, and the E_x peak becomes positive close to the source. Figure 2 shows that the InP-based MOSFET is more resistant to the field direction change than the Si-based MOSFET 5 nm below the gate and the peak of the longitudinal electric field E_x in the Si-based MOSFET is more than in the InP-based MOSFET. However, by increasing the dis-

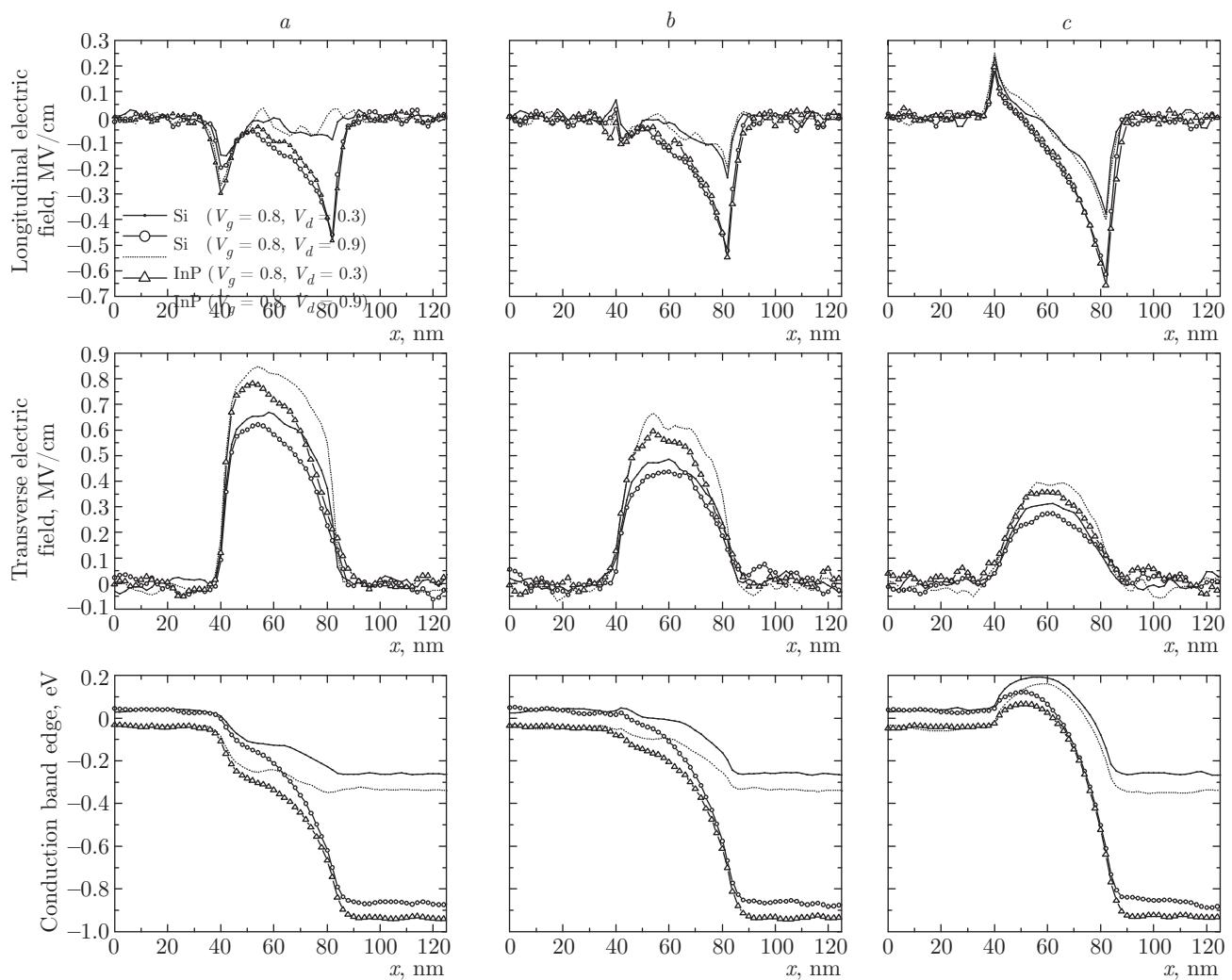


Fig. 2. Variation of the longitudinal and transverse electric fields and conduction band edge at two applied voltages; $V_g = 0.8$ V, $V_d = 0.3$ V, and 0.9 V, for Si- and InP-based MOSFETs at three positions 3 (a), 5 (b), 10 (c) nm below the gate

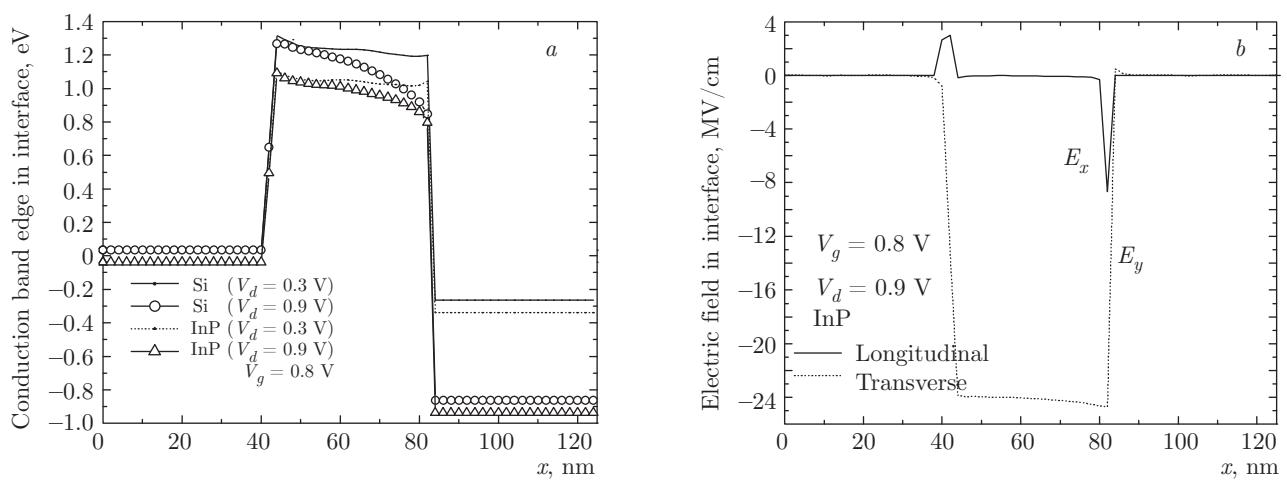


Fig. 3. Diagrams of (a) the conduction band edge and (b) electric fields in the device length (x -position) at the interface

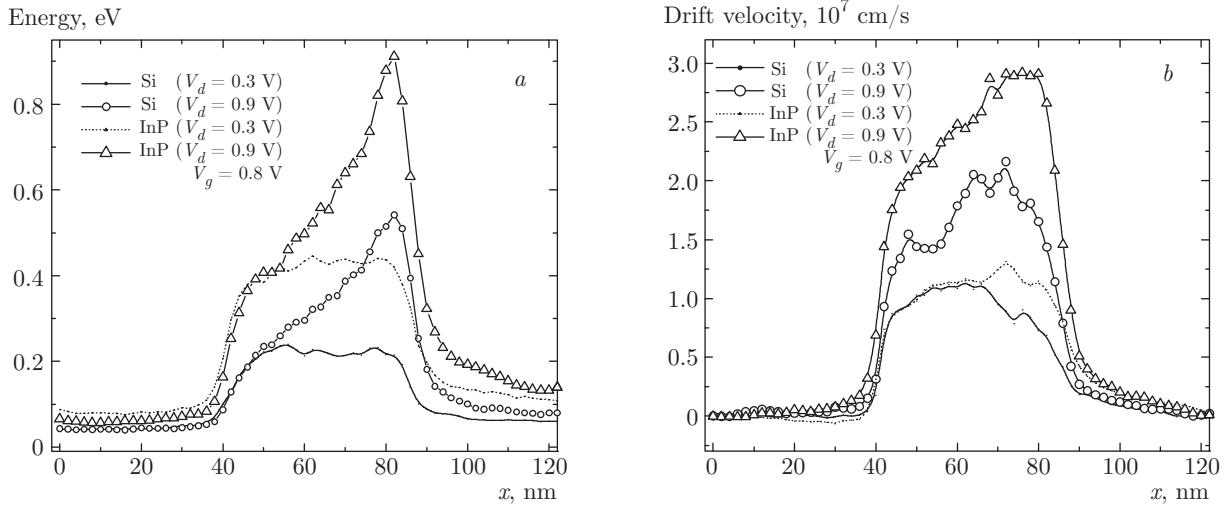


Fig. 4. (a) Average energy of electrons, (b) average velocity of electrons, in device in two applied voltages; $V_g = 0.8$ V, $V_d = 0.3$ V and $V_g = 0.8$ V, $V_d = 0.9$ V, for Si- and InP-based MOSFETs

tance from the gate, 10 nm under the gate, we see that E_x in the InP-based MOSFET is greater than in the Si-based MOSFET. Moreover, we found that the positive peak of E_x is reduced with increasing the drain voltage V_d near the source and the negative peak of E_x is increased with increasing V_d near the source.

Since the longitudinal electric field effect near the drain is related to V_d , it was found that E_x is positive near the drain at a low drain voltage ($V_d = 0.1$ V) and this peak in the InP-based MOSFET is more than in the Si-based MOSFET. However, E_x has a negative peak near the drain at higher drain voltages ($V_d \geq 0.3$). But the E_x peak in the Si-based MOSFET is more than in the InP-based MOSFET at $V_d = 0.3$ V and at higher drain voltages ($V_d \geq 0.5$ V), the negative peak of E_x in the InP-based MOSFET is greater than in the Si-based MOSFET (in fact it has a sharper pick).

Figure 2 for the transverse electric field (E_y) shows that the transverse electric field effect is reduced with receding from the gate and also increasing the drain voltage. It has been found that E_y in the InP-based MOSFET is greater than the Si-based MOSFET at all times.

Finally, Fig. 2 shows that the conduction band edge is lower in the area close to the gate and the electron transport possibility is increased. Due to the lower value in the InP-based MOSFET, electron transport and therefore the probability of the electron presence increase in the channel compared with the Si-based MOSFET. The difference of the conduction band edge values in the source and the drain between InP and

Si-based MOSFETs is related to the difference of electrochemical potential in the source and the drain between InP and Si-based MOSFETs.

Figure 3 shows that the effective potential approach leads to high electric fields at the interface. This leads to an upward shift of the conduction band edge. Figure 3a shows that the conduction band edge at the interface and under the effect of the effective potential approach in the Si-based MOSFET is more than in the InP-based MOSFET.

Figure 3b shows that the effective potential approach at the interface leads to a high negative transverse electric field. Moreover, the longitudinal electric field has a sharp positive peak near the source and has a sharp negative peak near the drain, with these sharp peaks being in nonequilibrium conditions.

Figure 4a shows that the average energy of electrons is approximately constant in all areas of the channel at $V_d = 0.3$ V. But the average energy of electrons increases as the drain voltage is increased and has a peak near the drain. We found that this value at ($V_d = 0.9$ V, $V_g = 0.8$ V) for the InP-based MOSFET is by about 0.2 eV greater than in the Si-based MOSFET.

Figure 4b shows that at $V_d = 0.3$ V and $V_g = 0.8$ V, the average velocity of electrons in Si and InP-based MOSFETs does not show the overshoot velocity. But with increasing the drain voltage, electrons show the overshoot velocity. At $V_d = 0.9$ V, electrons show the overshoot velocity for the Si-based MOSFET all along the channel and for the InP-based MOSFET from the middle of the channel toward the drain.

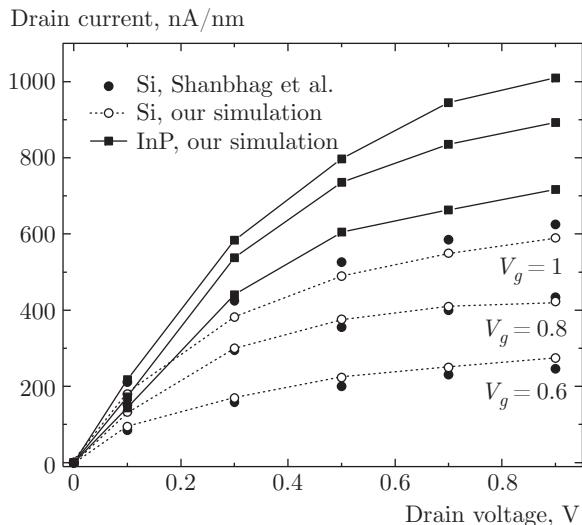


Fig. 5. I_d - V_d characteristics. Values reported in [31] (solid circles). Our simulation for Si-based MOSFET (dotted lines with open circles). Our simulation for InP-based MOSFET (black squares)

Figure 5 shows the diagram of the voltage-current feature for InP- and Si-based MOSFETs at three gate voltages of 0.6, 0.8, and 1 V. Figure 5 shows that for the Si-based MOSFET, our simulation results are in good agreement with theoretical and experimental results in [38].

4. CONCLUSION

EMC device simulation with quantum effect taken into account has been used to study electron transport properties in Si-based MOSFET. We used InP as a new channel material and Al₂O₃ as a high- k oxide layer dielectric instead of Si-SiO₂ based MOSFETs and compared them. Our results show that the transverse electric field, the conduction band edge, the electron average velocity, and the electron average energy in the InP-based MOSFET are greater than in the Si-based MOSFET in all areas of the channel; but comparing E_x in Si- and InP-based MOSFETs, we see different behaviors in various areas and voltages. Due to the effective potential approach, we observed high electric fields at the interface; for InP, our simulation shows E_x equal to 2.9 MV/cm near the source and -8.6 MV/cm near the drain, and E_y equal to -24.6 MV/cm in the channel. The comparison of the drain currents shows that the InP-based MOSFET provides a substantially higher drain current than the Si-based MOSFET. In the case of the Si-based MOSFET, results for I_d are in

good agreement with the theoretical and experimental values.

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